AMENDMENTS TO THE CLAIMS

1. (Original) A monolithic semiconductor device comprising:

a semiconductor substrate;

a plurality of upright free-standing microstructures formed over the substrate; and

a brace transversely extending between lateral sides of at least two of the free-standing microstructures.

2. (Original) The semiconductor device according to claim 1, wherein the brace interconnects substantially all of the microstructures.

3. (Original) The semiconductor device according to claim 1, where the brace is located substantially near upper ends of the microstructures.

4. (Original) The semiconductor device according to claim 1, wherein the brace has a width approximately equal to or less than the largest cross-sectional dimension of the microstructures.

5. (Original) The semiconductor device according to claim 1, wherein the brace comprises a microbridge structure extending above the substrate and between two or more of the microstructures.

6. (Original) The semiconductor device according to claim 1, where the microstructures each comprise a conductor material portion

standing upright over the substrate, and wherein the brace interconnects the conductor material portions of two or more of the microstructures.

7. (Original) The semiconductor device according to claim 1, wherein the microstructures comprise generally cylindrical container shapes and the brace comprises a microbridge structure.

8. (Original) The semiconductor device according to claim 1, wherein the microstructures comprise generally solid cylindrical shapes and the brace comprises a microbridge structure.

9. (Original) The semiconductor device according to claim 1, where the brace comprises a dielectric material.

10. (Original) The semiconductor device according to claim 1, further comprising a dielectric layer between the substrate and the brace, where the brace is vertically spaced from the dielectric layer.

11. (Original) The semiconductor device according to claim 1, wherein the microstructures comprise conductive material and the brace comprises a dielectric.

12. (Original) The semiconductor device according to claim 1, wherein the microstructures are defined within an active circuit area, and further comprising a die having non-active circuit areas located adjacent the active circuit area, wherein the brace further interconnects at least two of the microstructures with non-active areas of the die.

13. (Original) The semiconductor device according to claim 1, wherein the microstructures are stud capacitors.

14. (Original) The semiconductor device according to claim 1, wherein the microstructures are container capacitors.

15. (Original) The semiconductor device according to claim 1, wherein the microstructures comprise double-sided container capacitors.

16. through 22. (Cancelled)

23. (Currently Amended) <u>A semiconductor storage capacitor, comprising:</u>

<u>a semiconductor substrate;</u>

<u>a plurality of upright free-standing capacitor storage node microstructures formed over the substrate; and</u>

<u>a brace transversely extending between lateral sides of at least two of the free-standing microstructures</u> [[The semiconductor storage capacitor according to claim 16]], wherein the microstructures comprise generally solid cylindrical shapes and the brace comprises a microbridge structure.

24. through 27. (Cancelled)

28. (Currently Amended) <u>A semiconductor storage capacitor, comprising:</u>

<u>a semiconductor substrate;</u>

a plurality of upright free-standing capacitor storage node microstructures formed over the substrate; and

a brace transversely extending between lateral sides of at least two of the free-standing microstructures [[The semiconductor storage capacitor according to claim 16]], wherein the microstructures [[are]] comprise stud capacitors.

29. through 38. (Cancelled)

39. (Currently Amended) A memory circuit, comprising:

a semiconductor substrate having a memory cell including diffusion regions;

a dielectric layer on the substrate;

conductive plugs extending vertically from an upper surface of the dielectric layer to respective diffusion regions;

a plurality of upright free-standing capacitor storage node microstructures each formed over the dielectric layer and a respective conductive plug; and

a brace transversely extending between and laterally supporting respective lateral sides of at least two of the free-standing microstructures [[The memory circuit according to claim 31]], wherein the microstructures comprise generally solid cylindrical shapes and the brace comprises a microbridge structure.

40. through 43. (Cancelled)

44. (Currently Amended) A memory circuit, comprising:

a semiconductor substrate having a memory cell including diffusion regions;

a dielectric layer on the substrate;

conductive plugs extending vertically from an upper surface of the dielectric layer to respective diffusion regions;

a plurality of upright free-standing capacitor storage node microstructures each formed over the dielectric layer and a respective conductive plug; and

a brace transversely extending between and laterally supporting respective lateral sides of at least two of the free-standing microstructures [[The memory circuit according to claim 31]], wherein the microstructures [[are]] comprise stud capacitors.

45. and 46. (Cancelled)

47. (Original) A method of making a monolithic semiconductor device, comprising:

providing a substrate;

forming a plurality of upright free-standing microstructures formed over the substrate; and

forming a brace transversely extending between lateral sides of at least two of the free-standing microstructures.

48. (Original) The method according to claim 47, further comprising the steps of:

forming a dielectric layer on the substrate prior to forming the microstructures; and

and forming a conductive plug extending vertically through the dielectric layer from an active region in the substrate to a bottom of a microstructure.

49. (Original) The method according to claim 47, wherein the forming of the microstructures comprises forming generally cylindrical shapes, and the forming of the brace comprises forming a microbridge structure.

50. (Original) The method according to claim 47, further comprising forming a dielectric layer between the substrate and the brace, where the forming of the brace comprises forming the brace as vertically spaced from the dielectric layer.

51. (Original) The method according to claim 47, further comprising at least three upright free-standing microstructures braced transversely between lateral sides thereof by the brace.

52. (Original) A method of fabricating a capacitor, comprising the steps of:

forming a first dielectric layer over a substrate;

forming first and second contact holes through the first dielectric layer exposing the substrate;

filling the first and second contact holes with a conductive material to form respective first and second plugs;

forming a second dielectric layer having a top surface over the first dielectric layer;

forming a first via hole and a second via hole through the second dielectric layer exposing the respective first and second plugs;

introducing a polysilicon layer into the first via hole and the second via hole to form respective first and second polysilicon microstructures, where the microstructures have outside surfaces;

forming a shallow trench in the top surface of the second dielectric, wherein the trench intersects the outside surfaces of both the first and second polysilicon microstructures;

filling the shallow trench with a third dielectric material, where the third dielectric is different from the second dielectric material;

selectively etching and removing the second dielectric layer and leaving the first and second polysilicon microstructures with the third dielectric layer attached therebetween forming a brace support;

forming a hemispherical grain film over the first and second polysilicon microstructures;

forming a capacitor dielectric layer over the hemispherical grain film; and

forming a top electrode over the capacitor dielectric layer.

53. (Original) The method according to claim 52, wherein the second dielectric layer comprises a first dielectric material and the third dielectric layer comprises a second dielectric material, wherein the first and second dielectric materials are different from each other.

54. (Original) The method according to claim 52, wherein the second dielectric layer comprises a BPSG layer and the third dielectric layer comprises a silicon nitride layer.

55. (Original) The method according to claim 52, wherein hemispherical grain film comprises conductively doped polysilicon.

56. (Original) The method according to claim 52, wherein the capacitor dielectric layer comprises a silicon nitride layer and the top electrode comprises a polysilicon layer.

57. (Original) The method according to claim 52, wherein the brace formed interconnects substantially all of the microstructures.

58. (Original) The method according to claim 52, where the brace formed is located substantially near upper ends of the microstructures.

59. (Original) The method according to claim 52, wherein the brace formed has a width approximately equal to or less than the largest cross-sectional dimension of the microstructures.

60. (Original) The method according to claim 52, wherein the brace formed comprises a microbridge structure extending above the substrate and between two or more of the microstructures.

61. (Original) The method according to claim 52, where the microstructures formed each comprise a conductor material portion standing upright over the substrate, and wherein the brace formed interconnects the conductor material portions of two or more of the microstructures.

62. (Original) The method according to claim 52, further comprising forming additional microstructures and wherein the microstructures formed are defined within an active circuit area, and providing a die having non-active circuit areas located adjacent the active circuit area, wherein the brace formed further interconnects at least two microstructures with non-active areas of the die.

63. (Original) A method of fabricating a double sided capacitor container, comprising the steps of:

forming a first dielectric layer over a substrate;

forming first and second contact holes through the first dielectric layer exposing the substrate;

filling the first and second contact holes with a conductive material to form respective first and second plugs;

forming a second dielectric layer having a top surface over the first dielectric layer;

forming a first via hole and a second via hole through the second dielectric layer exposing the respective first and second plugs;

lining the first via hole and the second via hole with a polysilicon layer to form respective first and second polysilicon cylindrical containers, each having inside and outside surfaces;

forming a shallow trench in the top surface of the second dielectric, wherein the trench intersects the outside surfaces of both the first and second polysilicon containers;

filling the shallow trench with a third dielectric material, where the third dielectric is different from the second dielectric material;

electively etching and removing the second dielectric layer and leaving the first and second polysilicon containers with the third dielectric layer attached therebetween forming a brace support;

forming a hemispherical grain film on the inside and outside surfaces of the first and second polysilicon containers;

forming a capacitor dielectric layer over the hemispherical grain film; and

forming a top electrode over the capacitor dielectric layer.

64. (Original) The method according to claim 63, wherein the second dielectric layer comprises BPSG and the third dielectric layer comprises silicon nitride.

65. (Original) The method according to claim 63, wherein hemispherical grain film comprises conductively doped poly.

66. (Original) The method according to claim 63, wherein the capacitor dielectric comprises silicon nitride and the top electrode comprises poly.

67. (Original) A method of fabricating a capacitor having studs, comprising the steps of:

forming a first dielectric layer over a substrate;

forming first and second contact holes through the first dielectric layer exposing the substrate;

filling the first and second contact holes with a conductive material to form respective first and second plugs;

forming a second dielectric layer having a top surface over the first dielectric layer;

forming a first via hole and a second via hole through the second dielectric layer exposing the respective first and second plugs;

filling the first via hole and the second via hole with a conductive material to form respective first and second studs;

removing conductive material present on the flat surfaces of the second dielectric layer;

forming a shallow trench in the top surface of the second dielectric, wherein the trench intersects the outside surfaces of both the first and second studs;

filling the shallow trench with a third dielectric material, where the third dielectric is different from the second dielectric material;

selectively etching and removing the second dielectric layer and leaving the first and second studs with the third dielectric layer attached therebetween forming a brace support;

forming a hemispherical grain film on the outside surfaces of the first and second studs;

forming a capacitor dielectric layer over the hemispherical grain film; and

forming a top electrode over the capacitor dielectric layer.

68. (Original) The method according to claim 67, wherein the second dielectric layer comprises BPSG and the third dielectric layer comprises silicon nitride.

69. (Original) The method according to claim 67, wherein hemispherical grain film comprises conductively doped poly.

70. (Original) The method according to claim 67, wherein the capacitor dielectric comprises silicon nitride and the top electrode comprises poly.

71. (Original) The method according to claim 67, wherein the studs comprise a conductive material selected from the group consisting of Al, Al-alloys, W, and doped polysilicon.

72. through 76. (Cancelled)

77. (Currently Amended) A processor system, comprising:

a processor; and

a memory circuit fabricated on a semiconductor chip communicating with the processor, said memory circuit comprising:

a semiconductor substrate having a memory cell including diffusion regions;

a dielectric layer on the substrate;

conductive plugs extending vertically from an upper surface of the dielectric layer to respective diffusion regions;

a plurality of upright free-standing capacitor storage node microstructures each formed over the dielectric layer and a respective conductive plug; and

a brace transversely extending between and laterally supporting respective lateral sides of at least two of the free-standing microstructures [[The processor system according to claim 74]], wherein the capacitor microstructures comprise[[s]] capacitor studs.